REMARKS

Claims 1-6 are all the claims pending in the application. Claims 1-6 have been amended, either to clarify the invention or to place claims into independent form.

Claim Objections/Minor Informalities

Claim 2 is objected to because there is no antecedent basis for "the reference clock". The Examiner suggests that the word "the" be changed to --a--. This change has been made, as seen in the amended claims.

Claim Rejections - 35 U.S.C. § 102

Claim 2 is rejected under 35 U.S.C. § 102(e) as being anticipated by Asada et al (6,483,791). This rejection is traversed for at least the following reasons.

In comparing the claimed invention to the teachings in Asada et al, the Examiner asserts that Asada et al illustrates in Fig. 46 a clock generator comprising a phase control means [1422] that receives a reference clock [chCLK], controls a phase of the inputted reference clock [chCLK] according to a variable setting condition at each clock cycle, which generates a phase controlled clock, wherein the phase control means varies the setting condition to spread a spectrum of the phase controlled clock output [Dclk(0),---, Dclk(m)] at said output.

In the previous Amendment, Applicants argued that Asada et al concerns an optical disk apparatus and that Fig. 40 illustrates an embodiment of a wave form decoder 14 which includes a change point timing generator 1407, as illustrated in Fig. 46. Applicants also argued that there is no teaching or suggestion in the disclosure related to Fig. 46, beginning at col. 2, line 37, with regard to the desirability or achievement of "spectrum spread modulation". Applicants noted that one input to the charge point timing generator 1407 is a channel clock chCLK and the other is a case packet signal CP, with the only output being a case packet trigger CP_trg. Thus, Applicants argued that the subject matter of claim 2 is not anticipated by Asada.

The Examiner replies that the phrase "spectrum spread modulation" is not in the claim and that the concept of spreading the spectrum is clearly disclosed by Asada et al with respect to the function of the variable delay line [1425] with multi-tapped outputs. Further, the Examiner rebuts the Applicants' argument that the chCLK signal is not a reference clock. The Examiner admits that Asada et al does not call chCLK a "reference clock" but considers such "reference clock" to be any signal that is mainly employed to carry out a comparing process. The Examiner notes that in this case, "chCLK is used as a referenced clock for a comparison performed by the phase detector [1422].

Applicants have made an amendment to the claim in order to emphasize the unique structure of the invention as illustrated in Fig. 1. In particular, that structure includes a DLL circuit 10, which comprises variable delay circuit 2, phase comparator 3, first charge pump 4, subtractor 6 and filter 5. It also includes a delay setting circuit 11 and a second charge pump 12. As explained at page 7, lines 1-8, the clock generator optionally may include an oscillator that is integrated with the DLL circuit 10.

Thus, since original claim 2 differs from claim 1 in excluding a specific reference to the oscillator, Applicants have amended the claim to specifically recite that the "phase control means" comprises a first charge pump and a second charge pump, wherein the second charge pump generates a delay control voltage corresponding to a set delay time.

Claim Rejections - 35 U.S.C. § 103

Claims 1 and 3-5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Asada et al (6,483,791) in view of Lofgren et al (4,922,141). This rejection is traversed for at least the following reasons.

The Examiner again repeats the basis for the rejection of these claims, noting that Asada et al fails to disclose an oscillator for generating a reference clock but looks to Lofgren for such oscillator. The Examiner finds it obvious to modify Asada on the basis of the teachings of Lofgren.

In the previous Amendment, Applicants argued that claim 3 is not met by the teachings of Asada because it does not describe a "phase difference of the phase control clock to the reference clock does not exceed a specific limit value defined by the reference clock cycle as a unit." The Examiner argues that Asada has a delay lock loop, which is well known for synchronizing a referenced clock signal [chCLK 1421] and a delayed clock signal [output of 1425], which is a "*lock acquisition process*". It involves increasing and decreasing the delay amount based on the referenced clock signal.

With regard to claim 4, the Examiner also does not agree with Applicants' argument that the control input is regulated according to a profile such that the phase difference of the phase controlled clock to the reference clock [chCLK] gradually increases and gradually decreases between an upper limit and the lower limit. Again, the Examiner refers to the *lock acquisition process* for such feature.

Finally, with regard to Applicants' arguments regarding claim 5, the Examiner notes that the Applicants admitted that its patentability is based solely on its dependence from claim 3, which is taught by the prior art references.

Applicants submit that the amendments to claim 1, which are similar to those made to claim 2, provide a clear basis for distinction.

Finally, in reviewing the claims in the course of our analysis, Applicants observed that the meaning of the phrase "*phase control means*" may need clarification as to precisely the components that the Applicants wish to be included in such "*phase control means*".

Claim 1 separately recites an oscillator and a *phase control means* which varies the setting condition to spread a spectrum of a phase controlled clock outputted at said output. Thus, with reference to Fig. 1, the *phase control means* would include the DLL 10, delay setting circuit 11, and second charge pump 12.

This would be consistent with the recitation in claim 3 that the *phase control means* includes a variable delay circuit (2) and a circuit that detects a delayed state in the variable delayed circuit (phase comparator 3, first charge pump 4). These are all part of the DLL circuit 10.

However, claim 5, which depends from claim 3, specifically recites the existence of a DLL circuit containing the variable delay circuit. At first glance, this would appear to be consistent with the inclusion of the DLL circuit in the *phase control means*. However, the remainder of claim 5 states that the DLL circuit and *phase control means* synthesize the control input to the variable delay circuit. This appears to suggest that the DLL circuit is separate from the *phase control means*.

Further, Applicants note that claim 6, which depends from claim 5, specifically recites that the DLL circuit uses a comparator and a first charge pump, while the (separate) *phase control means* uses a second charge pump. This again treats the DLL circuit as separate from the *phase control means*. However, the disclosure teaches that the *phase control means* should include the DLL circuit.

Thus, Applicants have amended these claims, including claim 6, which has been made independent on the basis of the Examiner's indication of allowability, in order to recite the invention with greater consistency and clarity.

Since the rejection is final, and these changes is not likely to be accepted by the Examiner without the filing of an RCE, Applicants are submitting this Amendment under 37 C.F.R. § 1.114(c) concurrently with the filing of an RCE.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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